IN THE CLAIMS

1. (Previously Presented) A bias circuit comprising:

a reference cell to generate a bias signal; and

a first component coupled to the reference cell to adjust the bias signal by replicating a thermal characteristic of a second component that may be coupled to the bias circuit;

wherein the reference cell includes a feedback loop to drive a pair of ΔV_{BE} transistors; and

wherein the first component is arranged in the feedback loop.

2. (Canceled)

3. (Original) A bias circuit according to claim 1 wherein the feedback loop comprises a current mirror coupled between the first component and the reference cell.

4. (Original) A bias circuit according to claim 3 wherein the current mirror is arranged to load the reference cell.

5. (Original) A bias circuit according to claim 1 wherein the first component comprises a transistor.

6. (Canceled)

7. (Original) A bias circuit according to claim 1 wherein the reference cell and the first component are coupled together at a summing node.

8. (Original) A bias circuit according to claim 1 further comprising a clamping circuit coupled to the reference cell.

9. (Previously Presented) A method comprising:

generating a bias signal with a reference cell having a feedback loop to drive a pair of ΔV_{BE} transistors;

adjusting the bias signal by replicating a thermal characteristic of a component that may be coupled to the bias circuit by operating a replica component in the feedback loop.

10. (Original) A method according to claim 9 wherein replicating the thermal characteristic comprises operating a replica component under similar operating conditions to the component that may be coupled to the bias circuit.

11. (Canceled)

12. (Previously Presented) A method according to claim 9 wherein operating a replica component in a feedback loop comprises mirroring current through the replica component into the reference cell.

13. (Original) A method according to claim 9 wherein adjusting the bias signal comprises summing a current from a replica component with a current from the reference cell.

14. (Original) A method according to claim 9 further comprising clamping a voltage of the reference cell.

15. (Previously Presented) A system comprising:

a first circuit comprising a reference cell to generate a bias signal, and a first component coupled to the reference cell; and

a second circuit coupled to the first circuit to receive the bias signal, the second circuit comprising a second component;

wherein the first component is arranged to adjust the bias signal by replicating a thermal characteristic of the second component;

wherein the reference cell includes a feedback loop to drive a pair of ΔV_{BE} transistors; and

wherein the first component is arranged in the feedback loop.

16. (Canceled)

17. (Original) A system according to claim 15 wherein the feedback loop comprises a current mirror coupled between the first component and the reference cell.

18. (Original) A system according to claim 15 wherein the reference cell and the first component are coupled together at a summing node.

19. (Original) A system according to claim 15 wherein the first and second components have a matching thermal characteristic.

20. (Previously Presented) A bias circuit comprising:

bias means for generating a bias signal, wherein the bias means comprises a feedback loop arranged to drive a pair of ΔV_{BE} transistors; and

replication means for replicating a thermal characteristic of a component that may be coupled to the bias circuit, wherein the replication means comprises a replication component that is matched to the component that may be coupled to the bias circuit;

wherein the replication component is arranged in the feedback loop.

21. (Canceled)

22. (Canceled)

23. (Original) A bias circuit according to claim 20 further comprising means for combining a signal from the bias means with a signal from the replication means.

24. (Original) A bias circuit according to claim 20 further comprising means for controlling the amount of compensation provided by the replication means.